Code No: 154AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester (Special) Examinations, January/February - 2021
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Convert the following:
i) $AB_{16}=(\ )_{10}$
ii) $1234_8=(\ )_{10}$
iii) $10110011_2=(\ )_{10}$
iv) $772_{10}=(\ )_{16}$
v) $(0.513)_{10}=(\ )_8$
b) Convert $(0011001.0101)_2$ to decimal and octal. [9+6]

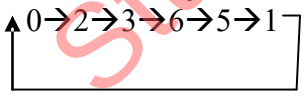
2.a) State and prove Conesus theorem.
b) Write the following binary numbers in signed 1's compliment form and 2's compliment form using 16-bit registers:
i)+1001010 ii)-11110000 iii)-11001100.1. [6+9]

3.a) Solve the following function using K-MAP
A=f(w,x,y,z)=π(1,2,3,4,8,9,10,11,12,13,14,15) and implement it using NOR gates only.
b) Explain Carry look ahead adder with a neat diagram. [9+6]

4.a) Solve the following function using K-MAP and implement it by using NAND gates
B=f(w,x,y,z)=∑(1,2,34,9)+∑d(10,11,12,13,14,15)
b) Explain how a decoder can be converted into a demultiplexer with relevant block diagram tables. [9+6]

5. Derive the Characteristic equation for listed flip-flops:
a) SR F/F b) JK F/F c) T F/F d) D F/F. [4+4+4+3]

6. Design a modulus Synchronous counter for the sequence using D Flip flop. [15]



7.a) Draw and explain the working principle of successive approximation ADC.
b) Enlist the advantages and disadvantages of dual slope ADC. [8+7]

8.a) Design a 3×8 decoder and implement using a suitable PLA.
b) Describe DRAM with an appropriate diagram and explain its timings. [8+7]

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